CLAIMS

What is claimed is:

1. A memory storage system that is accessed by a first central processing unit (CPU), comprising:

a line cache including a plurality of pages that are accessed by the first CPU; and

a first memory device that stores data that is loaded into said line cache when a miss occurs,

wherein when said miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one.

2. The memory storage system of claim 1 wherein when the first CPU requests data from an m^{th} page of said n pages in said line cache, wherein m is greater than one and less than or equal to n, said line cache loads p additional pages with data from sequential locations in said first memory device.

3. The memory storage system of claim 1 further comprising:

a second memory device; and

a line cache control system that controls data flow between said line cache, the first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with the first CPU, that receives a first program read request from the first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and loads said n pages of said line cache when said miss occurs.

4. The memory storage system of claim 3 further comprising:

a second CPU;

a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and

a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between the first CPU and said second CPU.

5. A memory storage system that is accessed by a first central processing unit (CPU), comprising:

a line cache including a plurality of pages that are accessed by the first CPU; and

a first memory device that stores data that is loaded into said line cache when a miss occurs,

wherein after an initial miss, said line cache prevents additional misses as long as the first CPU addresses sequential memory locations of said first memory device.

6. The memory storage system of claim 5 wherein when said miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one.

7. The memory storage system of claim 6 wherein when the first CPU requests data from an m^{th} page of said n pages in said line cache, wherein m is greater than one and less than or equal to n, said line cache loads p additional pages with data from sequential locations in said first memory device.

8. The memory storage system of claim 5 further comprising:

a second memory device; and

a line cache control system that controls data flow between said line cache, the first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with the first CPU, that receives a first program read request from the first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and loads said n pages of said line cache when said miss occurs.

9. The memory storage system of claim 8 further comprising:

a second CPU;

a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and

a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between the first CPU and said second CPU.

10. A memory storage system, comprising:

a line cache including a plurality of pages;

a first central processing unit (CPU) that accesses data stored in said line cache; and

a first memory device that stores data that is loaded into said line cache when a miss occurs,

wherein when said miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one, and wherein when said first CPU requests data from an m^{th} page of said n pages in said line cache, wherein m is greater than one and less than or equal to n, said line cache loads p additional pages with data from sequential locations in said first memory device.

11. The memory storage system of claim 10 further comprising:

a second memory device; and

a line cache control system that controls data flow between said line cache, said first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with said first CPU, that receives a first program read request from said first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and retrieves said n pages of line cache when said miss occurs.

12. The memory storage system of claim 11 further comprising:

a second CPU;

a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and

a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between said first CPU and said second CPU.

13. A memory storage system, comprising:

a line cache including a plurality of pages;

a first central processing unit (CPU) that accesses said pages of said line cache; and

a first memory device that stores data that is loaded into said line cache when a miss occurs,

wherein after an initial miss, said line cache prevents additional misses as long as said first CPU addresses sequential memory locations of said first memory device.

14. The memory storage system of claim 13 wherein when said miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one.

15. The memory storage system of claim 14 wherein when said first CPU requests data from an m^{th} page of said n pages in said line cache, wherein m is greater than one and less than or equal to n, said line cache loads p additional pages with data from sequential locations in said first memory device.

16. The memory storage system of claim 13 further comprising:

a second memory device; and

a line cache control system that controls data flow between said line cache, said first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with said first CPU, that receives a first program read request from said first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and loads said n pages of said line cache when said miss occurs.

17. The memory storage system of claim 16 further comprising:

a second CPU;

a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and

a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between said first CPU and said second CPU.